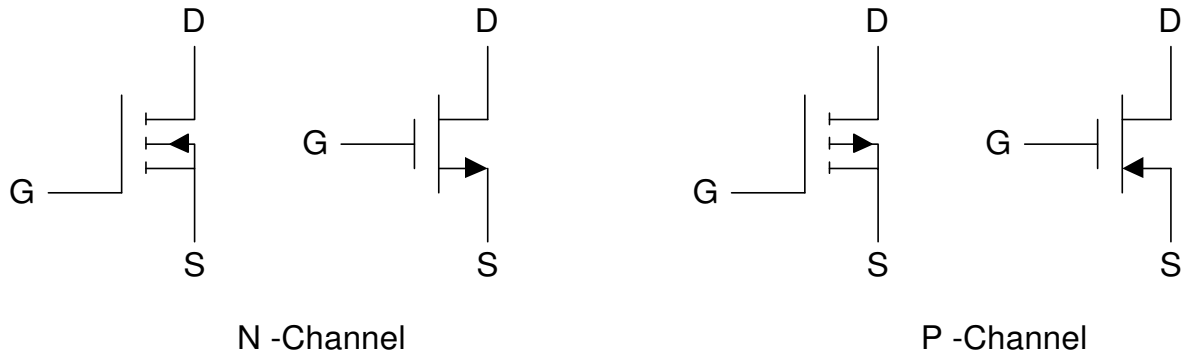
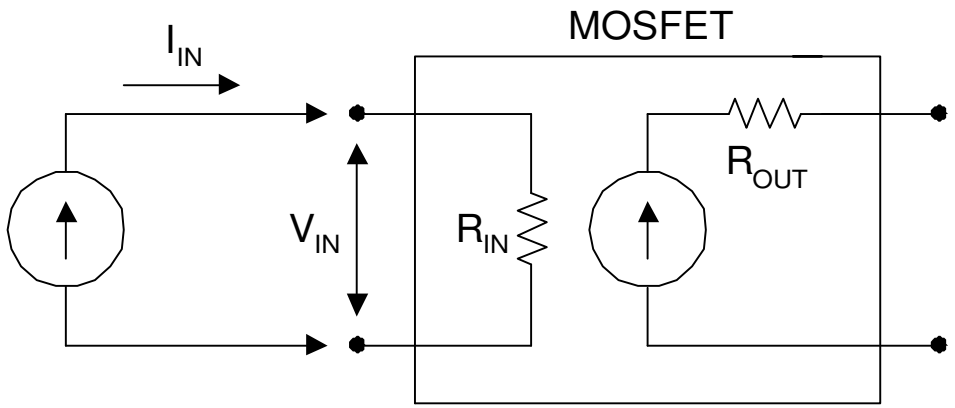
MOS dan CMOS



Gambar 1.11. Simbol MOSFET

Berbeda dengan TTL, rumpun ini menggunakan transistor jenis MOSFET (Metal Oxide Semiconductor Field Effect Transistor) sebagai piranti aktipnya. MOSFET ini terdiri dari N-Channel dan P-Channel.

Karena menggunakan efek medan maka impedansi masukan dari transistor ini sangat besar. Oleh karena itu transistor ini sangat peka terhadap muatan listrik statis.



Gambar 1.12. Rangkaian ekivalen MOSFET

Untuk sebarang nilai R_{IN} maka besarnya tegangan masukan V_{IN} adalah

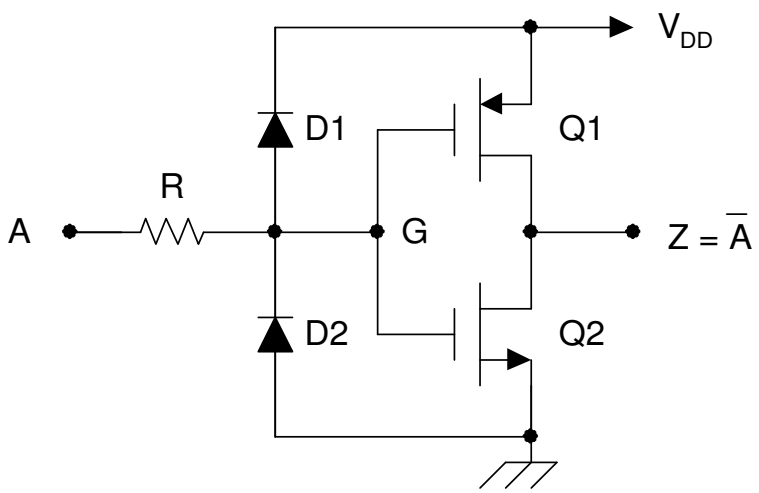
$$V_{IN} = I_{IN} \times R_{IN}$$

Jika $R_{IN} = \infty$ maka

$$V_{IN} = I_{IN} \times \infty$$
$$= \infty$$

Tegangan masukan yang terlalu besar akan merusak isolasi gate dari transistor. Oleh karena itu rangkaian masukan dari transistor ini harus diproteksi.

Proteksi Masukan

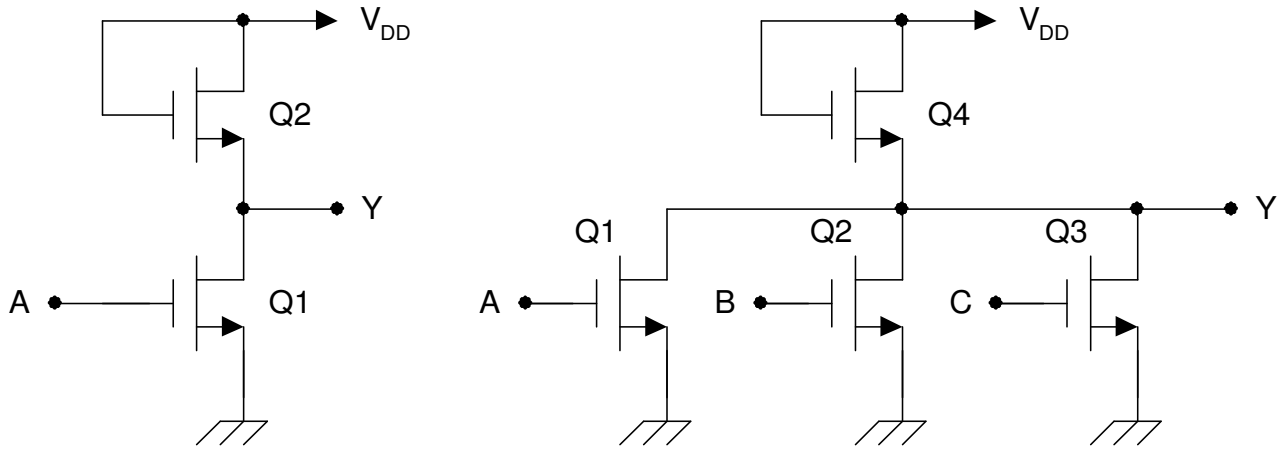


Untuk memproteksi masukan gerbang dari tegangan lebih yang disebabkan oleh lucutan muatan statis, digunakan rangkaian proteksi yang umumnya terdiri dari tahanan sebagai pembatas arus dan dioda sebagai pembatas tegangan.

Dioda D1 dan D2 berfungsi sebagai clamping dioda. Jika tegangan masukan > V_{DD} maka D1 akan menghantar sehingga tegangan G akan dibatasi sebesar $V_{DD} + V_F$.

Jika tegangan masukan < GND maka D2 akan mengahntar sehingga tegangan G akan dibatasi sebesar –0,7V.

Contoh-contoh Rangkaian dengan MOSFET



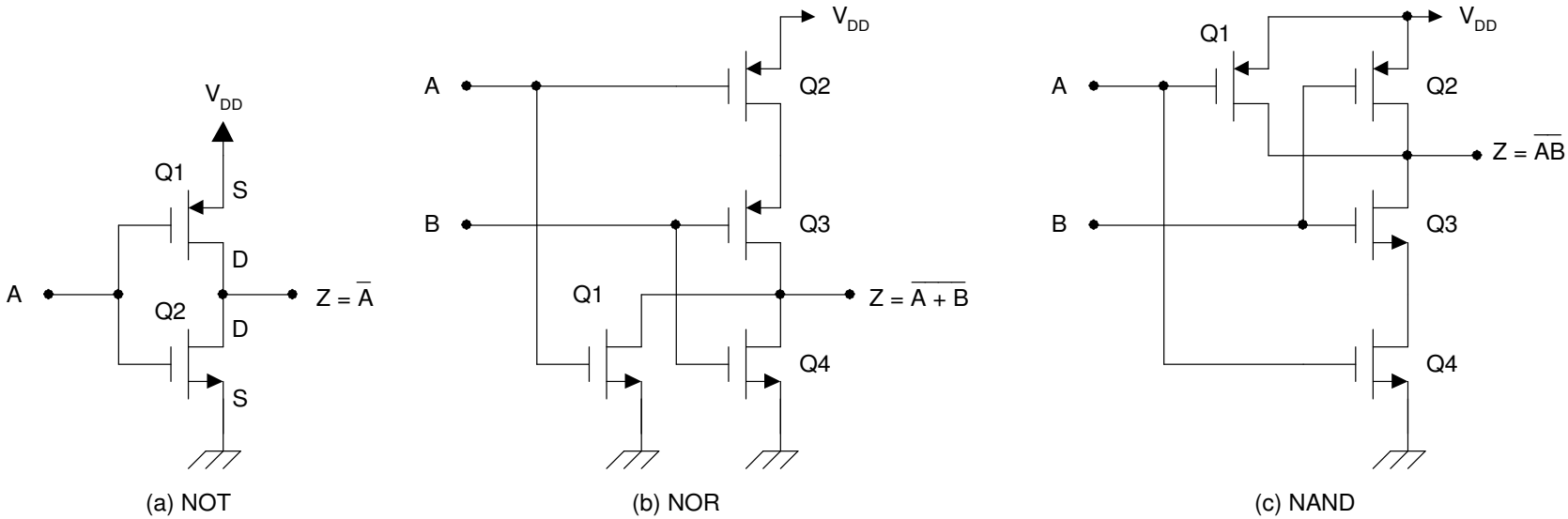
(a) Gerbang NOT

(b) Gerbang NOR

Pada gambar (a) transistor Q2 berfungsi sebagai sumber arus konstan (pengganti tahanan. Besarnya tegangan Y ditentukan oleh konduktansi transistor Q1.

Pada gambar (b) transistor Q4 yang berfungsi sebagai sumber arus konstan. Tegangan Y akan tinggi jika Q1, Q2 dan Q3 tidak menghantar.

Contoh-contoh rangkaian dengan CMOS



Disini digunakan transistor komplemen. Pada gambar (a) transistor Q1 adalah jenis PMOS sedangkan transistor Q2 adalah jenis NMOS. Jika tegangan A rendah maka Q1 menghantar dan Q2 menyumbat sehingga tegangan Z akan tinggi.

Sebaliknya jika tegangan A tinggi maka Q1 menghantar dan Q2 menyumbat sehingga tegangan Z akan rendah.

Spesifikasi Standard

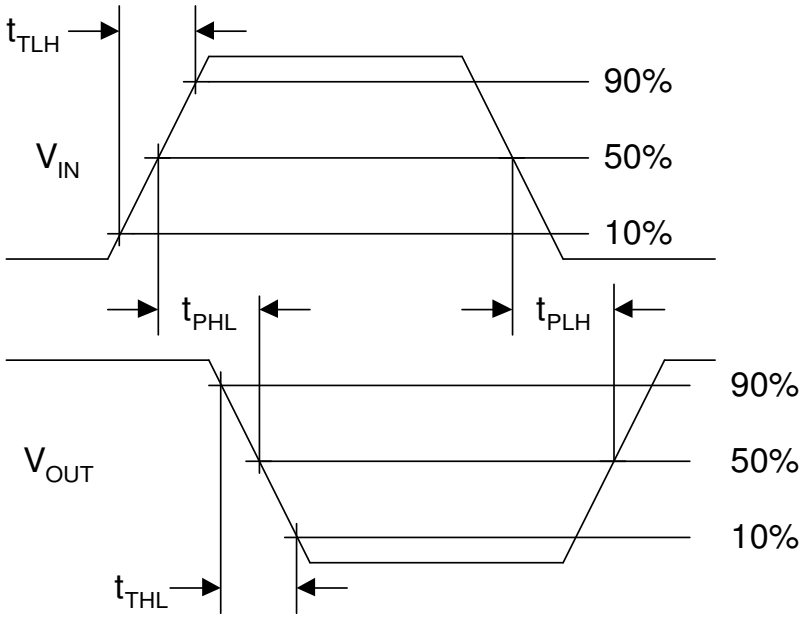
Rating Maksimum Absolut

Supply DC	V_{DD}	-0,5V sampai +18V_{DC}
Tegangan masukan	V_{IN}	-0,5V sampai V_{DD} + 0,5V_{DC}
Arus masukan DC	I_{IN}	±10 mA_{DC}
Temperatur penyimpanan	T_S	-65 sampai 150^{0}C

Kondisi Operasi Yang Dianjurkan

Supply DC	V_{DD}	+3V sampai +15VDC
Temperatur kerja	T_A	
Versi Militer		-55 sampai +125^{0}C
Versi Komersial		-40 sampai +85^{0}C

Delay Propagasi dan Delay Transien



Fungsi Membalik

Buffered dan Nonbuffered

CMOS terdiri dari dua jenis, yaitu :

- Buffered
- Nonbuffered

Jenis Buffered dilengkapi dengan penguat pada bagian keluarannya untuk meningkatkan kemampuannya

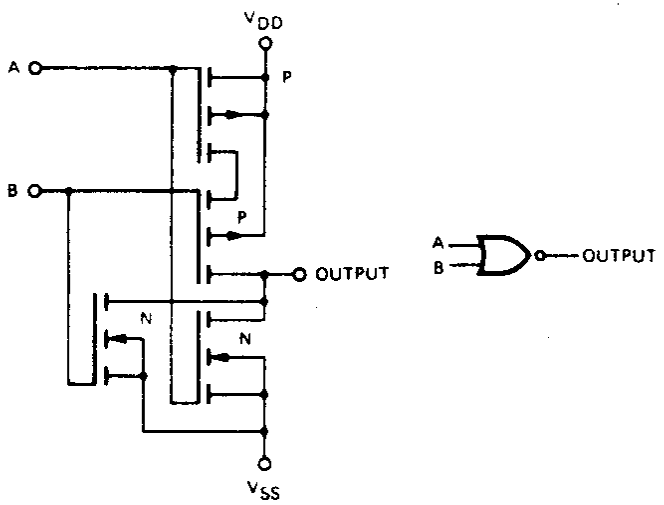


Fig. 4-2. CONVENTIONAL NON-BUFFERED 2-INPUT NOR GATE

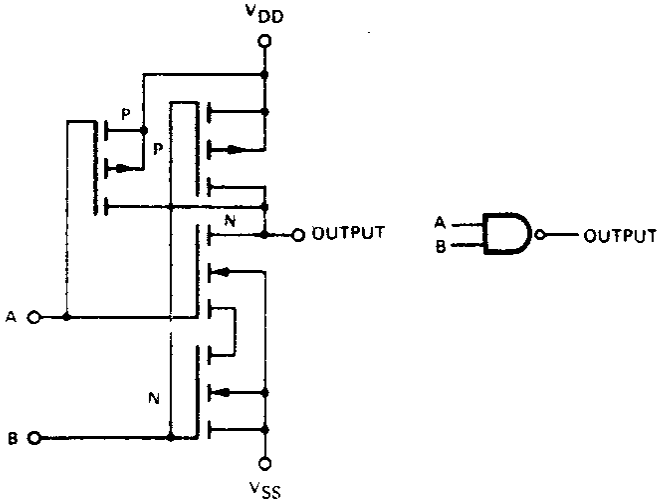


Fig. 4-3. CONVENTIONAL NON-BUFFERED 2-INPUT NAND GATE

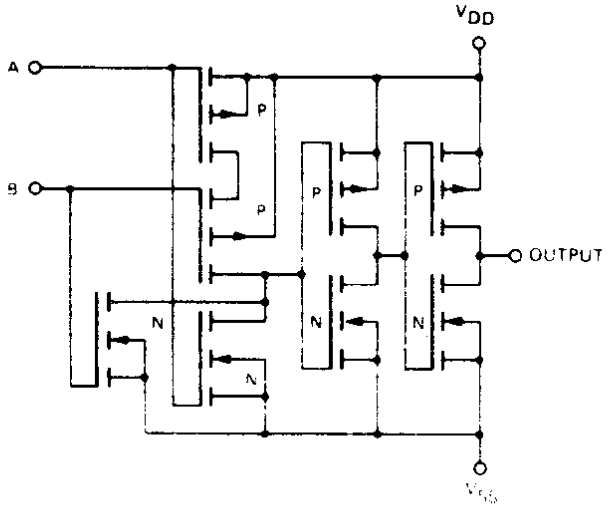


Fig. 4-4. FAIRCHILD 4001B FULLY BUFFERED NOR GATE

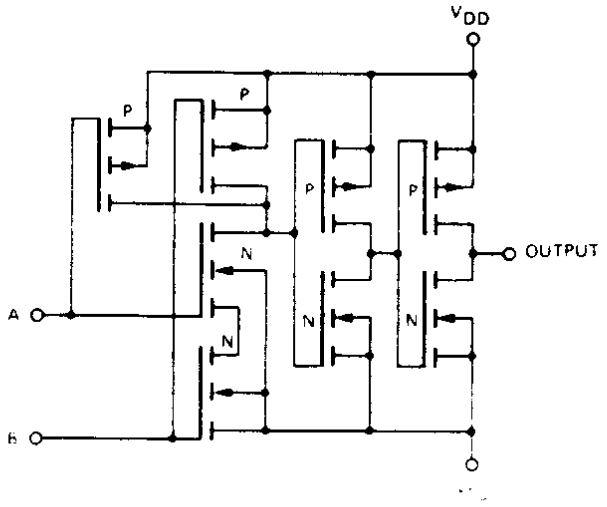


Fig. 4-5. FAIRCHILD 4011B FULLY BUFFERED NAND GATE

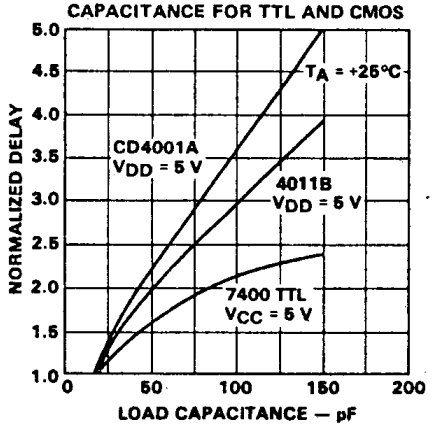
Perbandingan CMOS dengan keluarga lain

PARAMETER	STANDARD TTL	74L	DTL	LOW POWER SCHOTTKY	FAIRCHILD 4000B CMOS 5 V SUPPLY	FAIRCHILD 4000B CMOS 10 V SUPPLY
PROPAGATION DELAY (GATE)	10 ns	33 ns	30 ns	5 ns	40 ns	20 ns
FLIP-FLOP TOGGLE FREQUENCY	35 MHz	3 MHz	5 MHz	45 MHz	8 MHz	16 MHz
QUIESCENT POWER (GATE)	10 mW	1 mW	8.5 mW	2 mW	10 nW	10 nW
NOISE IMMUNITY	1 V	1 V	1 V	0.8 V	2 V	4 V
FAN OUT	10	10	8	20	50*	50*

*OR AS DETERMINED BY ALLOWABLE PROPAGATION DELAY

Fig. 5-1 CMOS COMPARED TO OTHER LOGIC FAMILIES

Fig. 5-3
NORMALIZED PROPAGATION DELAY VERSUS LOAD CAPACITANCE FOR TTL AND CMOS



Pengaruh Beban Kapasitip terhadap Delay Propagasi

Fig. 5-4a
POSITIVE-GOING PROPAGATION
DELAY VERSUS LOAD CAPACITANCE

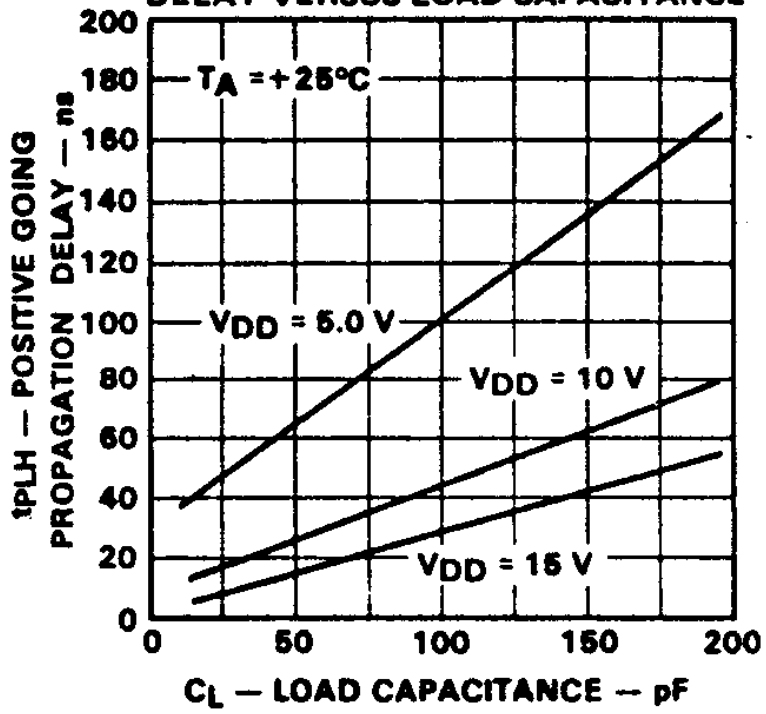
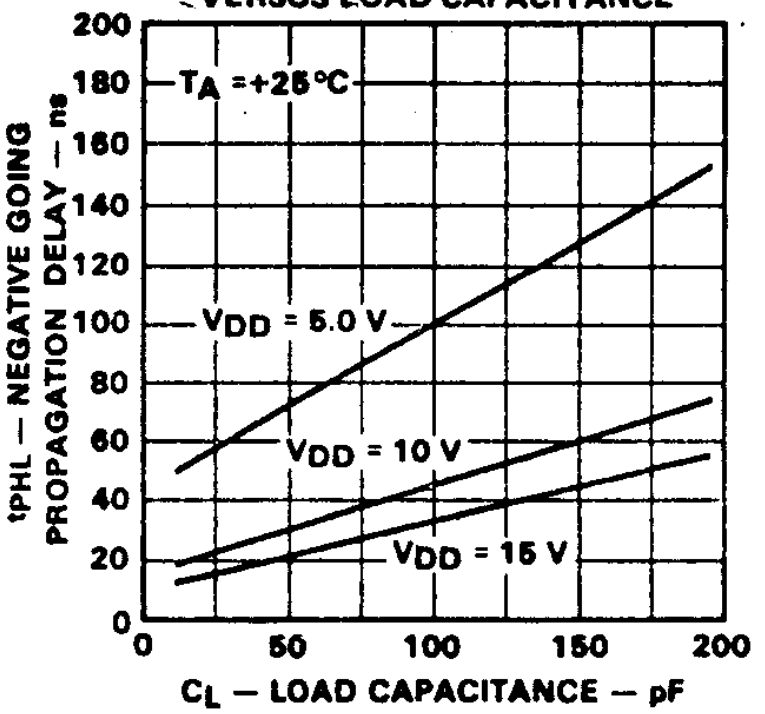


Fig. 5-4b
NEGATIVE-GOING
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



Pengaruh Tegangan catu pada delay propagasi

Fig. 5-5a
POSITIVE-GOING PROPAGATION
DELAY VERSUS POWER SUPPLY VOLTAGE

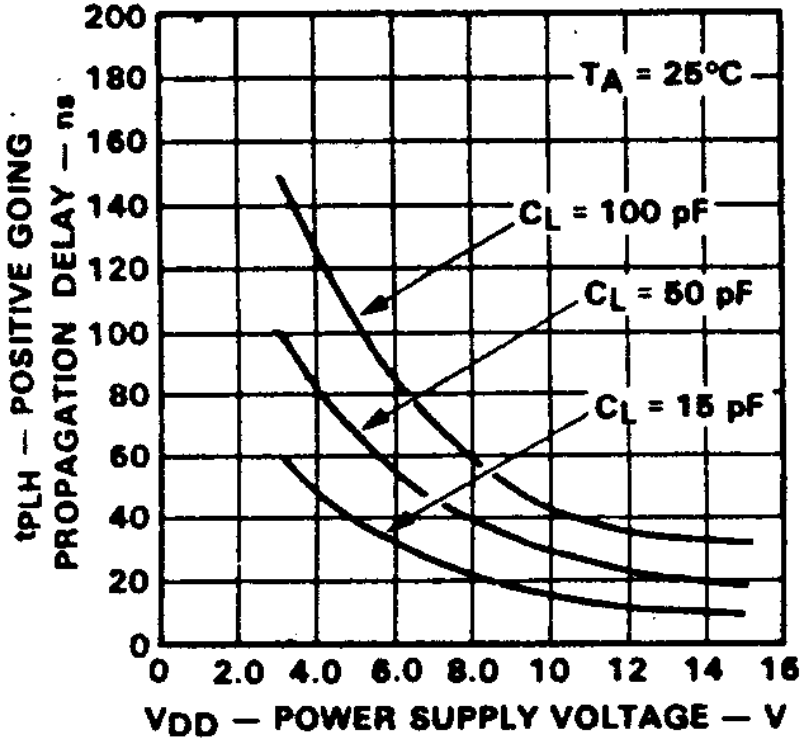
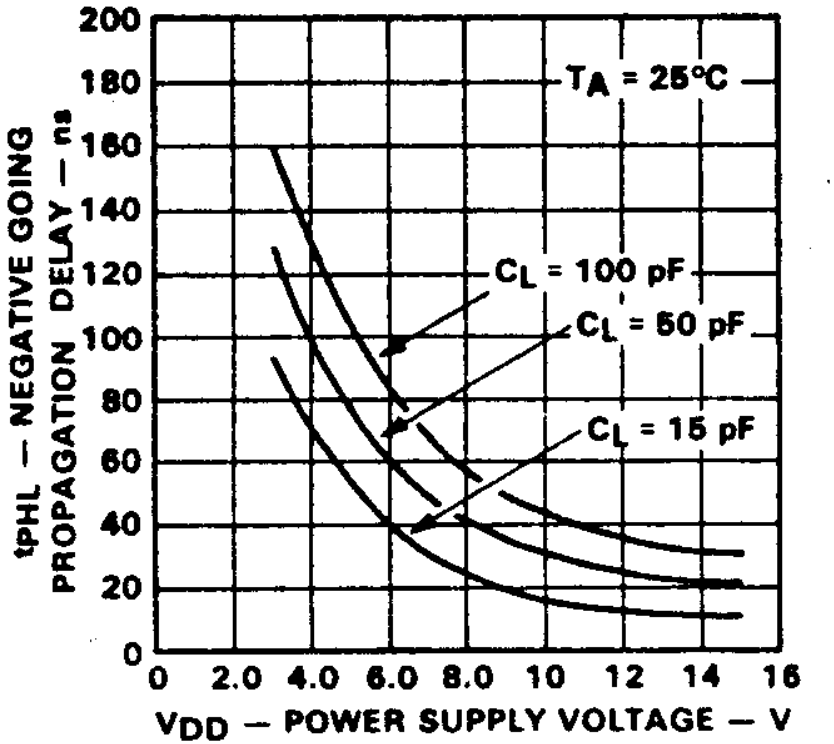


Fig. 5-5b
NEGATIVE-GOING PROPAGATION
DELAY VERSUS POWER SUPPLY VOLTAGE



4001 dan 4002

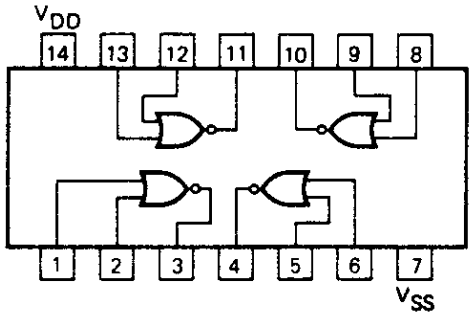
4001B

4002B

QUAD 2-INPUT NOR GATE • DUAL 4-INPUT NOR GATE

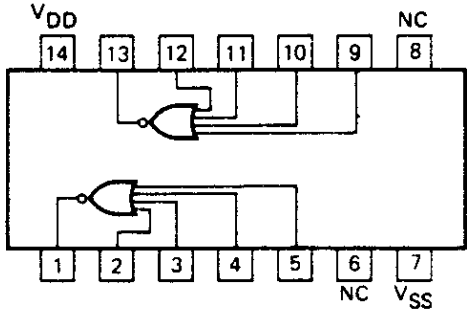
DESCRIPTION – These CMOS logic elements provide the positive input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

4001B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

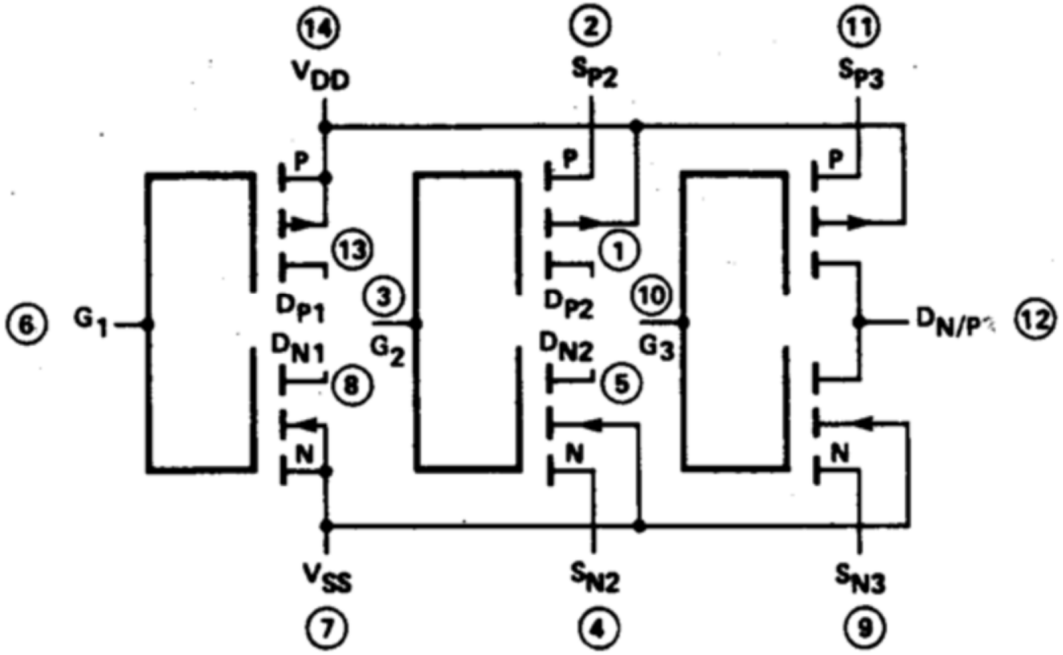


NOTE:
The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-line Package.

4002B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



CD4007 Dual Complementary Pair plus Inverter



CONNECTION DIAGRAM
DIP (TOP VIEW)

NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

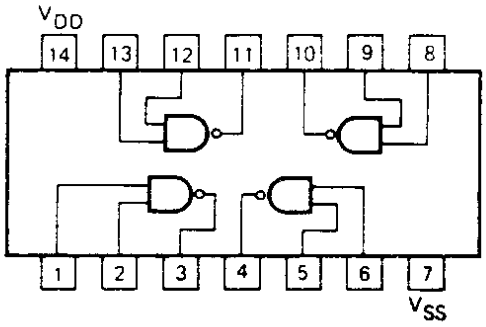
4011B • 4012B

4011B QUAD 2-INPUT NAND GATE

4012B DUAL 4-INPUT NAND GATE

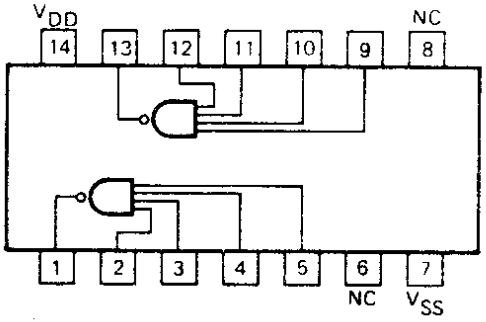
DESCRIPTION – These CMOS logic elements provide the positive input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

4011B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-line Package.

4012B
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



4013 Dual D Flip-flop

SYNCHRONOUS INPUTS		OUTPUTS	
CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
⎍	L	L	H
⎍	H	H	L

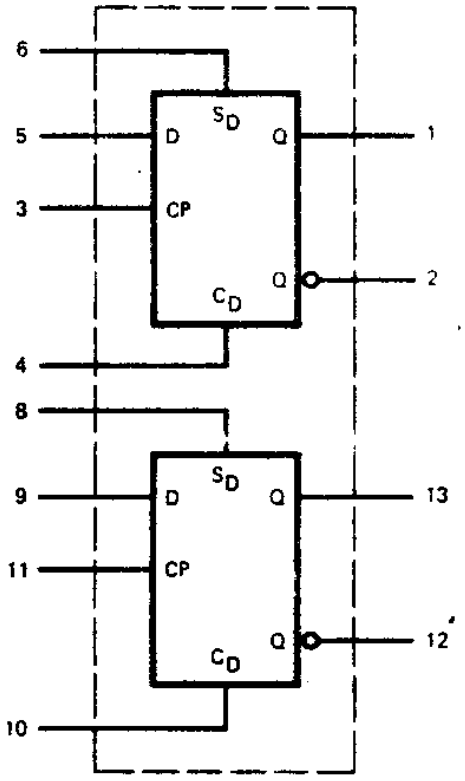
Conditions: $S_D = C_D$ = LOW

ASYNCHRONOUS INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
H	H	H	H

L = LOW Level
H = HIGH Level
⎍ = Positive-Going Transition
Q_{n+1} = State After Clock Positive Transition

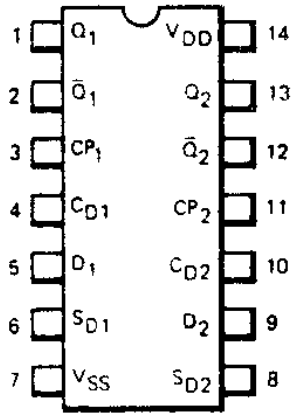
LOGIC SYMBOL

4013B



V_{DD} = Pin 14
V_{SS} = Pin 7

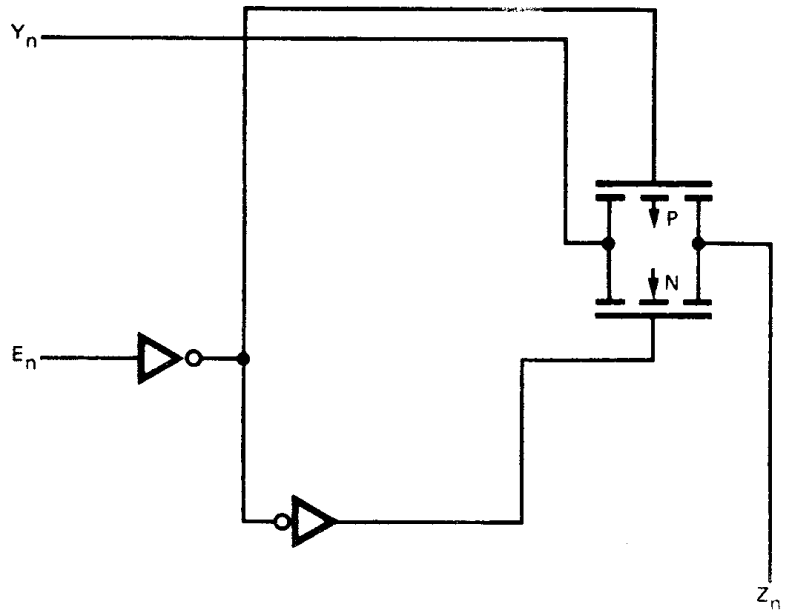
CONNECTION DIAGRAM
DIP (TOP VIEW)



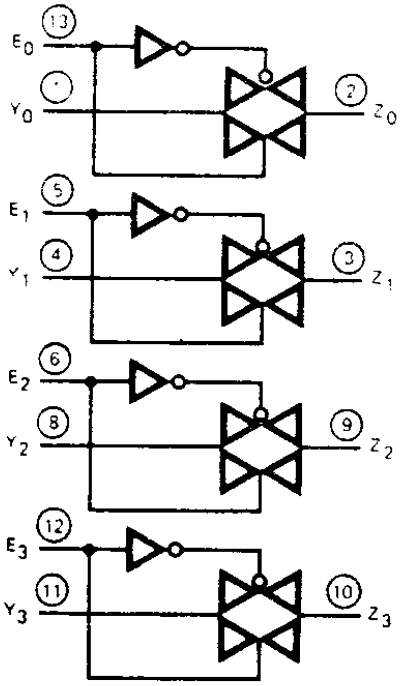
4016 Quad Bilateral Switch

Setiap kemasan mengandung empat buah analog switch. Harus dijaga agar tegangan masukan selalu berkisar antara V_{DD} dan GND.

LOGIC DIAGRAM (1/4 of a 4016B)



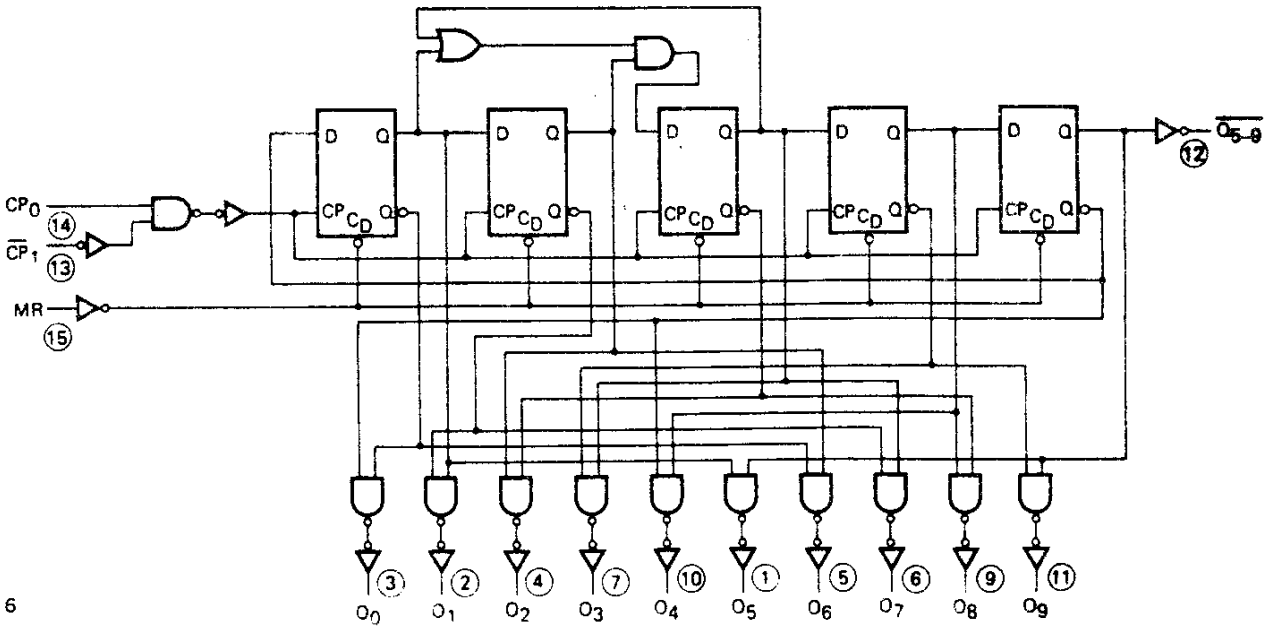
LOGIC SYMBOL



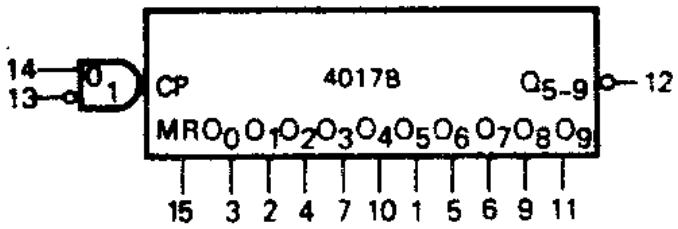
VDD = Pin 14
VSS = Pin 7
○ = Pin Numbers

4017

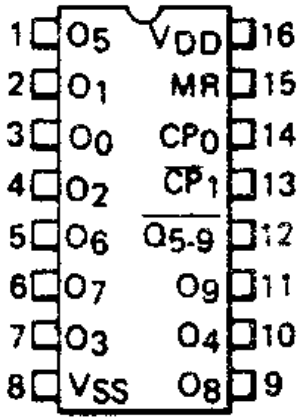
LOGIC DIAGRAM



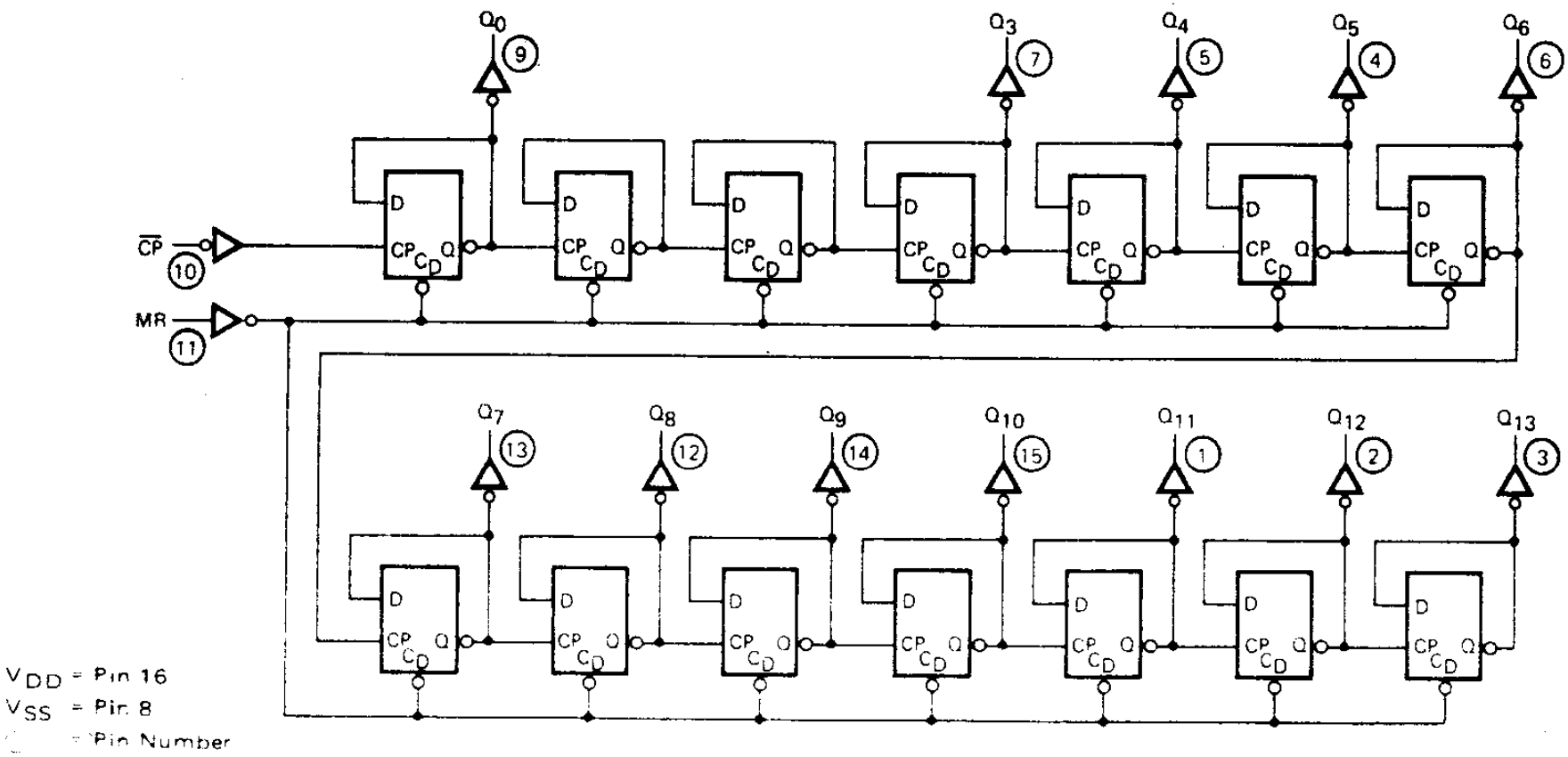
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

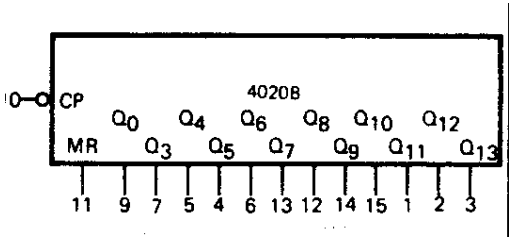


V_{DD} = Pin 16
V_{SS} = Pin 8



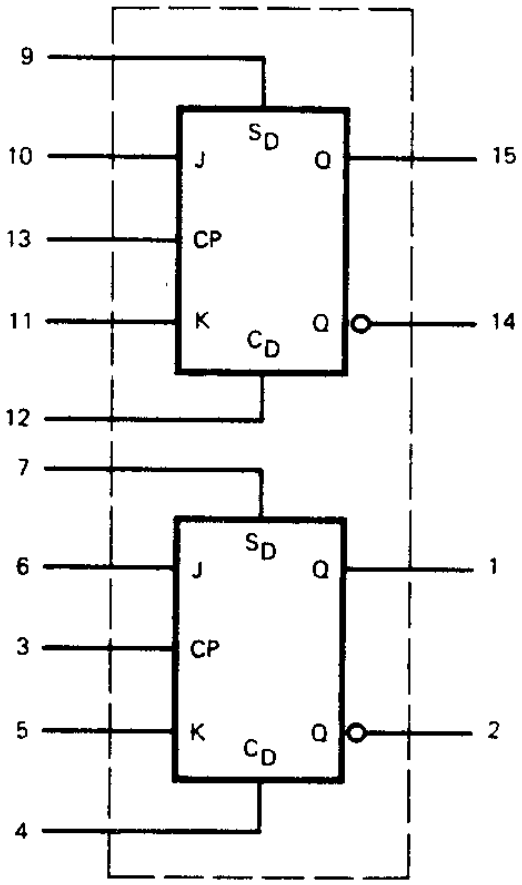
4020 14 Stage Binary Counter





4026 Dual JK Flip-flop

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

ASYNCHRONOUS INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
H	H	H	H

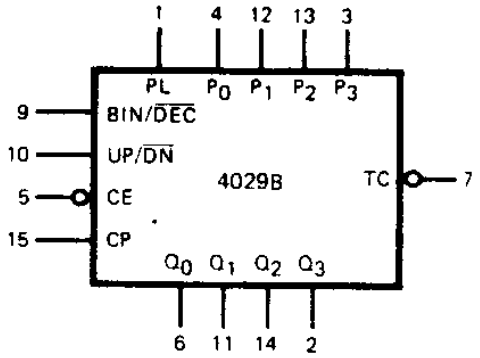
L = LOW Level
H = HIGH Level
⌐¬ = Positive-Going Transition
Q_{n+1} = State After Clock Positive Transition

SYNCHRONOUS INPUTS			OUTPUTS	
CP	J	K	Q_{n+1}	$\overline{Q}_{n+1}$
⌐¬	L	L	NO CHANGE	
⌐¬	H	L	H	L
⌐¬	L	H	L	H
⌐¬	H	H	$\overline{Q}_n$	Q_n

Conditions: $S_D = C_D$ = LOW

4029 Synchronous Up/Down Counter

LOGIC SYMBOL

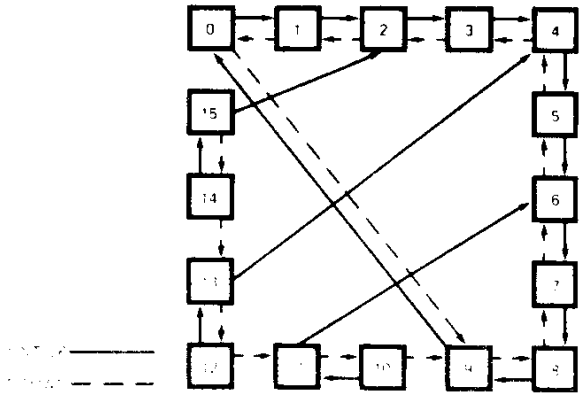


V_{DD} = Pin 16
V_{SS} = Pin 8

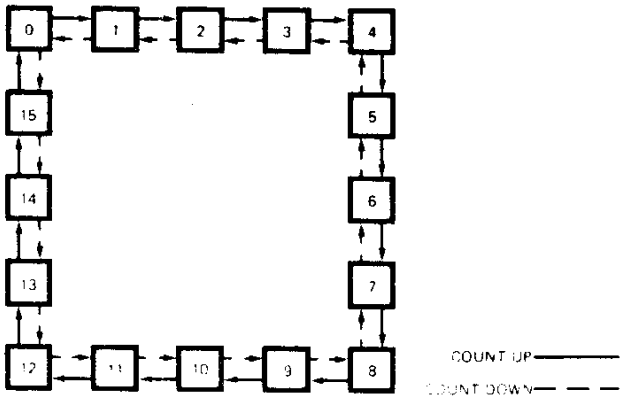
MODE SELECTION TABLE

PL	BIN/$\overline{DEC}$	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	X	H	X	No Change
L	L	L	L	⎍	Count Down, Decade
L	L	H	L	⎍	Count Up, Decade
L	H	L	L	⎍	Count Down, Binary
L	H	H	L	⎍	Count Up, Binary

4029B STATE DIAGRAM, BIN/$\overline{DEC}$ = LOW



4029B STATE DIAGRAM, BIN/$\overline{DEC}$ = HIGH



LOGIC EQUATION FOR TERMINAL COUNT

$$TC = CE \bullet [UP \bullet Q_0 \bullet Q_3 \bullet (\overline{BIN} + (Q_1 \bullet Q_2)) + (\overline{UP} \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)]$$

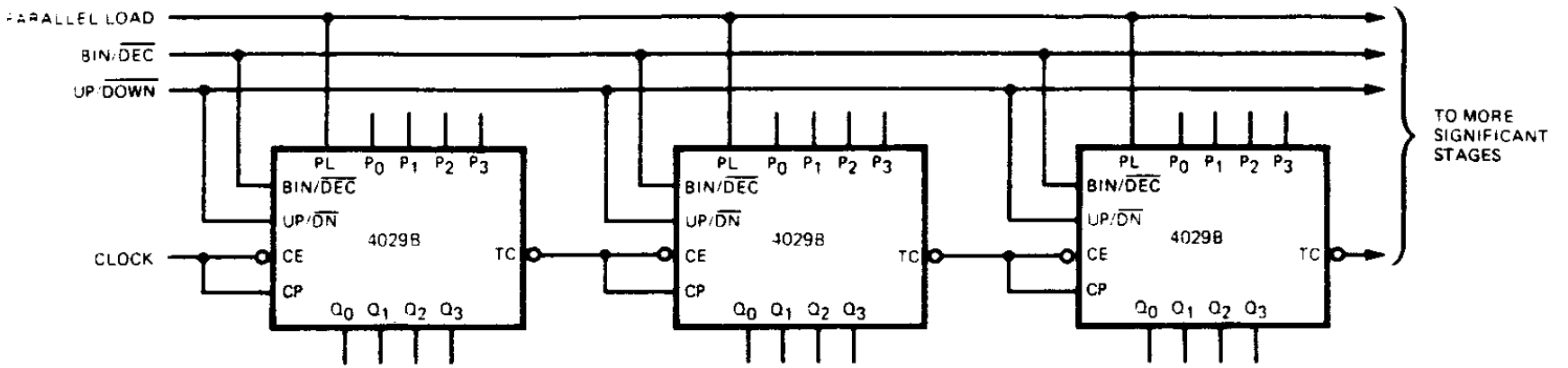


Fig. 1 RIPPLE CLOCK EXPANSION

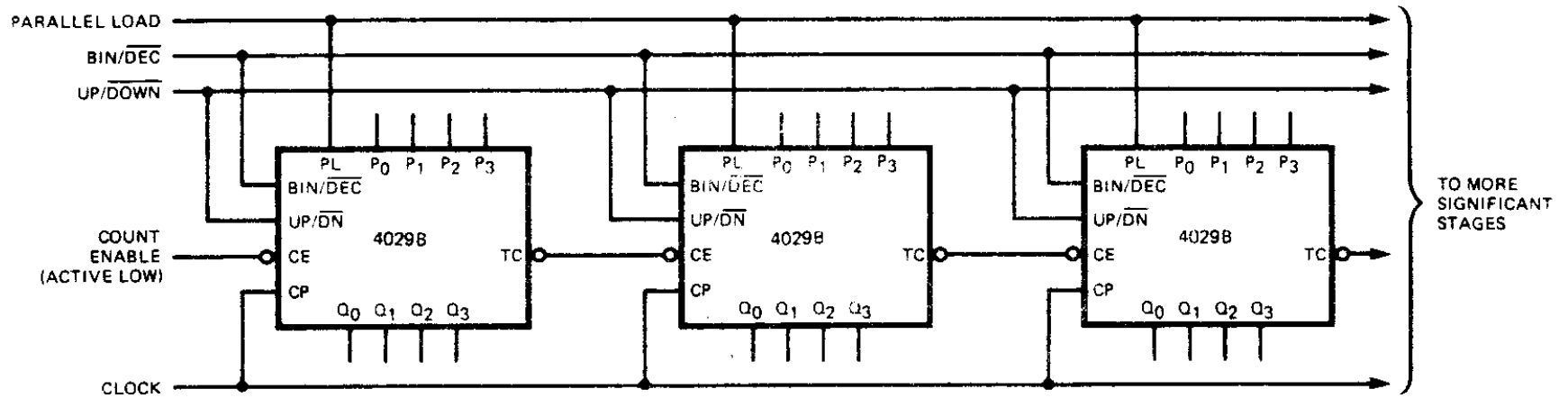


Fig. 2 PARALLEL CLOCK EXPANSION (FULLY SYNCHRONOUS)

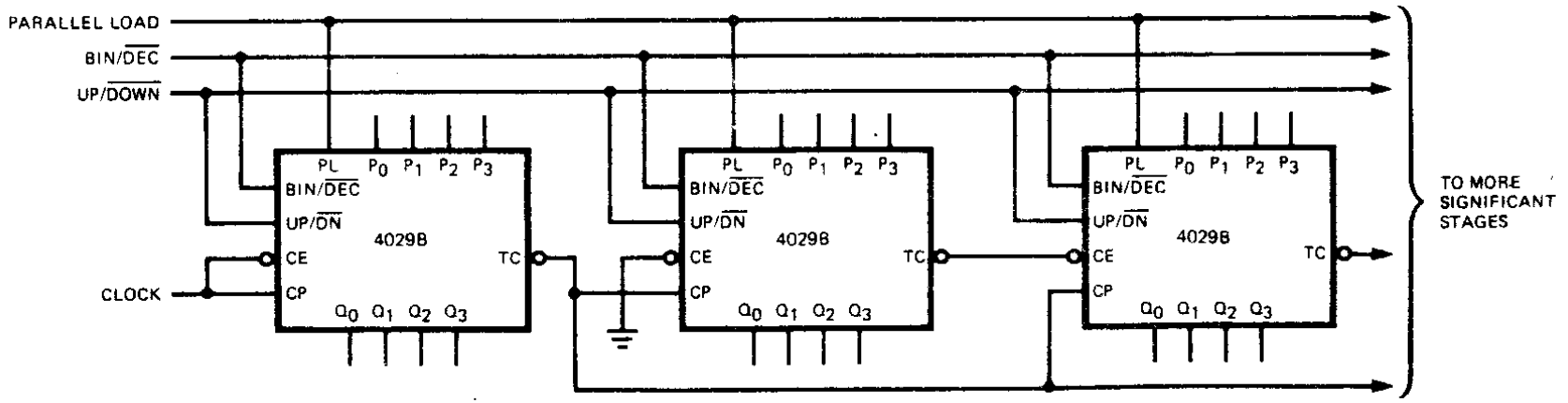


Fig. 3 SEMI-SYNCHRONOUS EXPANSION

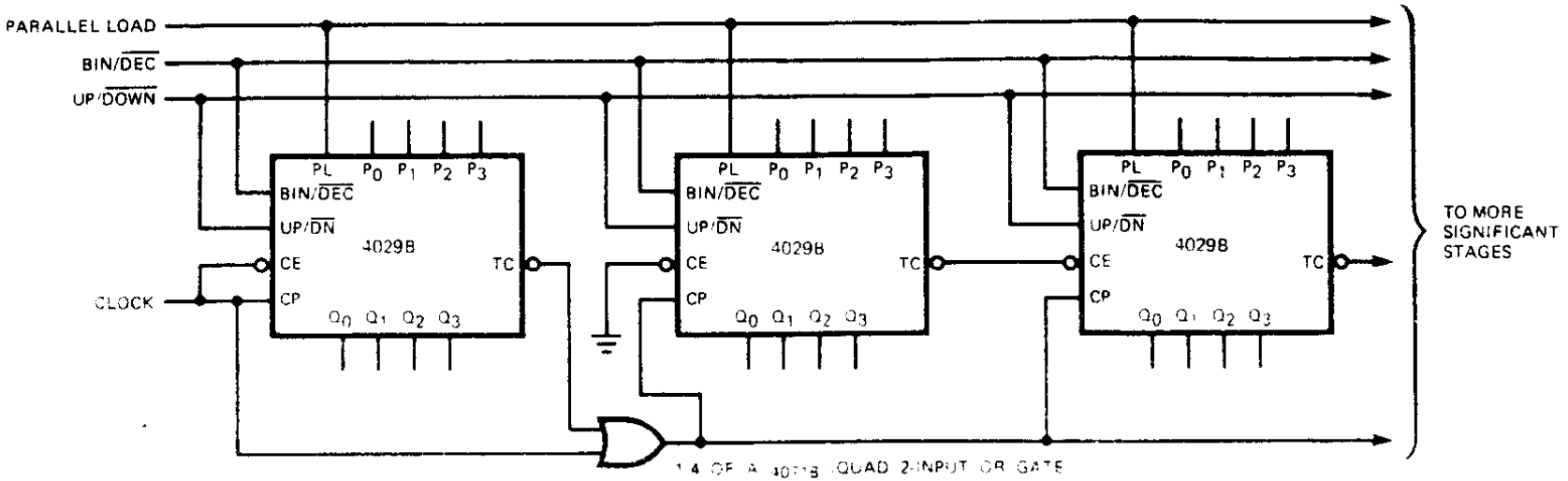
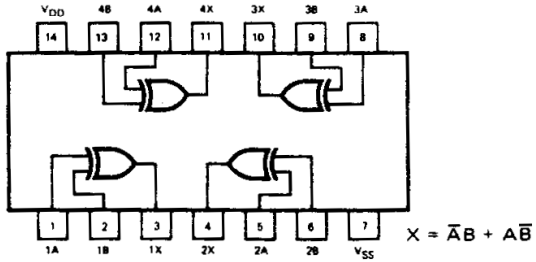


Fig 4 HIGH SPEED SEMI-SYNCHRONOUS EXPANSION

4070B/74C86/54C86

QUAD EXCLUSIVE-OR GATE

DESCRIPTION – The 4070B CMOS logic element provides the Exclusive-OR function. The outputs are fully buffered for best performance. The 4070B is a direct replacement for the 74C86/54C86.



LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

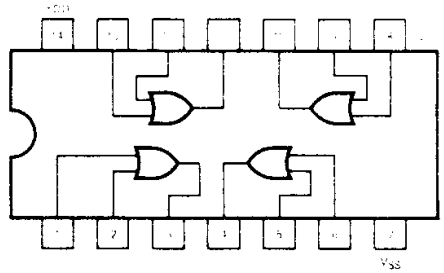
NOTE:
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

4071B

QUAD 2-INPUT OR GATE

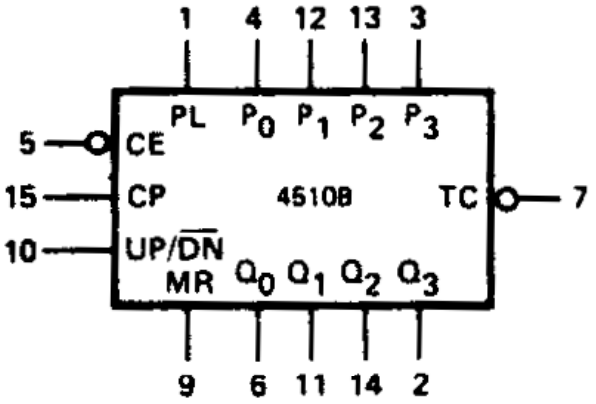
DESCRIPTION – The 4071B is a positive logic Quad 2-Input OR Gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

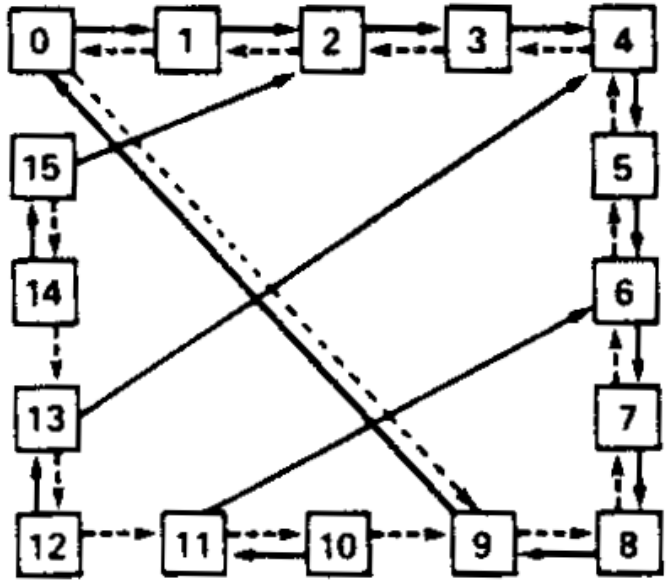
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

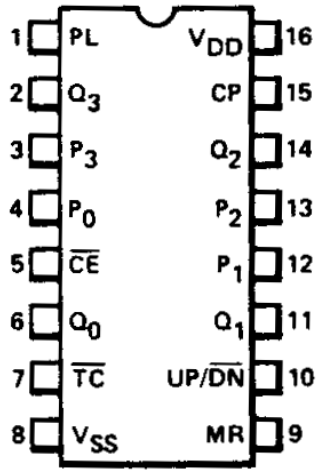


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

4510 Presettable Up/Down Decade Counter







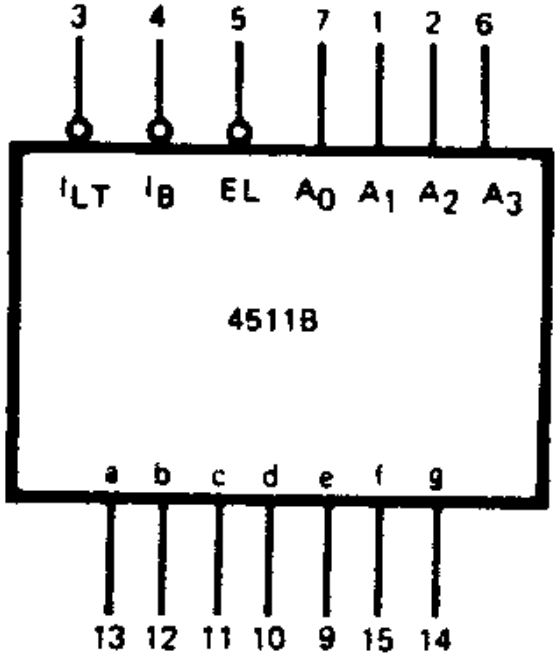
MODE SELECTION TABLE

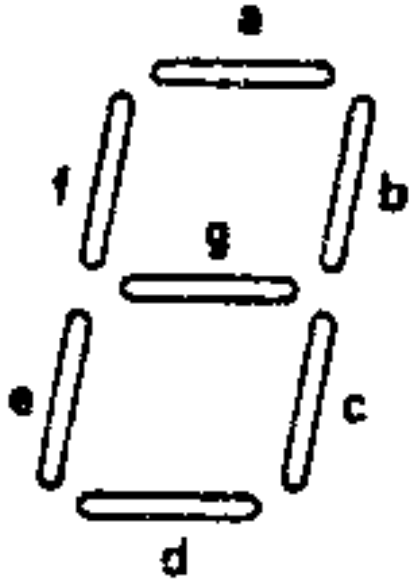
PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	H	X	No Change
L	L	L	⌐	Count Down, Decade
L	H	L	⌐	Count Up, Decade

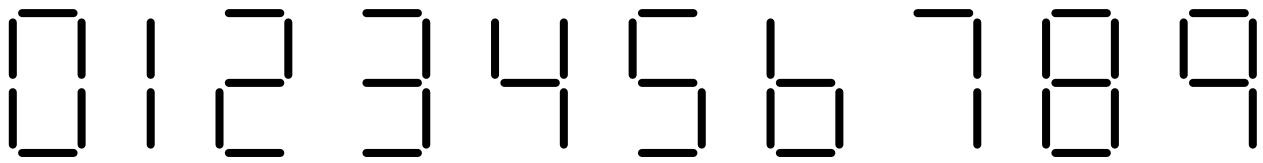
MR = LOW
H = HIGH Level
L = LOW Level

X = Don't Care
⌐ = Positive-Going Transition

4511 BCD to 7-segment latch/decoder/driver





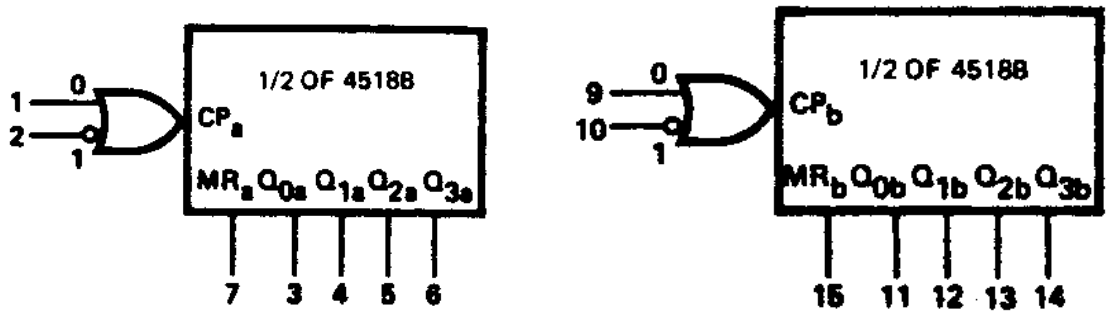


TRUTH TABLE

INPUTS							OUTPUTS							
$\overline{EL}$	$\overline{I_B}$	$\overline{I_{LT}}$	A_3	A_2	A_1	A_0	a	b	c	d	e	f	g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	L	H	H	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	H	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	H	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X				•				•

H = HIGH Level
L = LOW Level
X = Don't Care
• = Depends upon the BCD code applied during the LOW-to-HIGH transition of $\overline{EL}$

4518 Dual BCD Counter



1/2 OF A 4518B LOGIC DIAGRAM